Lab 5 Report

# Part 1 – Ripple Carry Adder (RCA)

## Design Files for RCA

### RCA\_4bits



### full\_adder



### register\_logic



## Test-bench for RCA



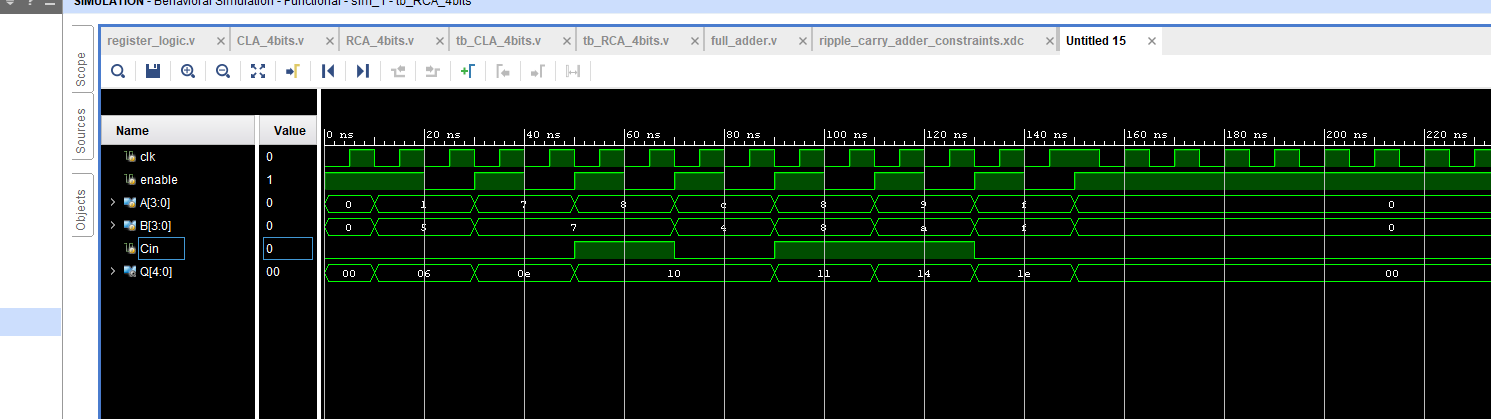
## Testcases Table for RCA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A[3:0] | B[3:0] | Cin | Sum[3:0] | Cout |
| 0001 | 0101 | 0 | 0110 | 0 |
| 0111 | 0111 | 0 | 1110 | 0 |
| 1000 | 0111 | 1 | 0000 | 1 |
| 1100 | 0100 | 0 | 0000 | 1 |
| 1000 | 1000 | 1 | 0001 | 1 |
| 1001 | 1010 | 1 | 0100 | 1 |
| 1111 | 1111 | 0 | 1110 | 1 |

## Constraints File for RCA



## Simulation Waveform for RCA TB



# Part 2 – Carry Lookahead Adder (CLA)

## and Equations

## Design Files for CLA

### CLA\_4bits



### register\_logic



## Test-bench for CLA



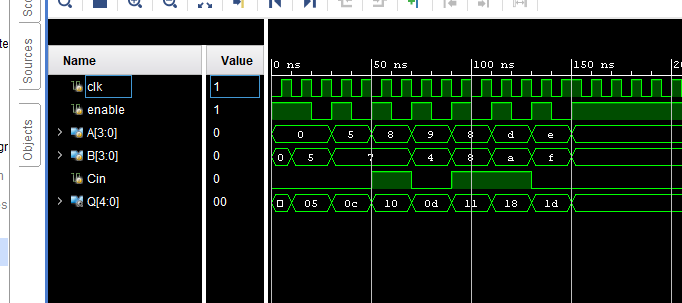
## Testcases Table for CLA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A[3:0] | B[3:0] | Cin | Sum[3:0] | Cout |
| 0000 | 0101 | 0 | 0101 | 0 |
| 0101 | 0111 | 0 | 1100 | 0 |
| 1000 | 0111 | 1 | 0000 | 1 |
| 1001 | 0100 | 0 | 1101 | 0 |
| 1000 | 1000 | 1 | 0001 | 1 |
| 1101 | 1010 | 1 | 1000 | 1 |
| 1110 | 1111 | 0 | 1101 | 1 |

## Constraints File for CLA



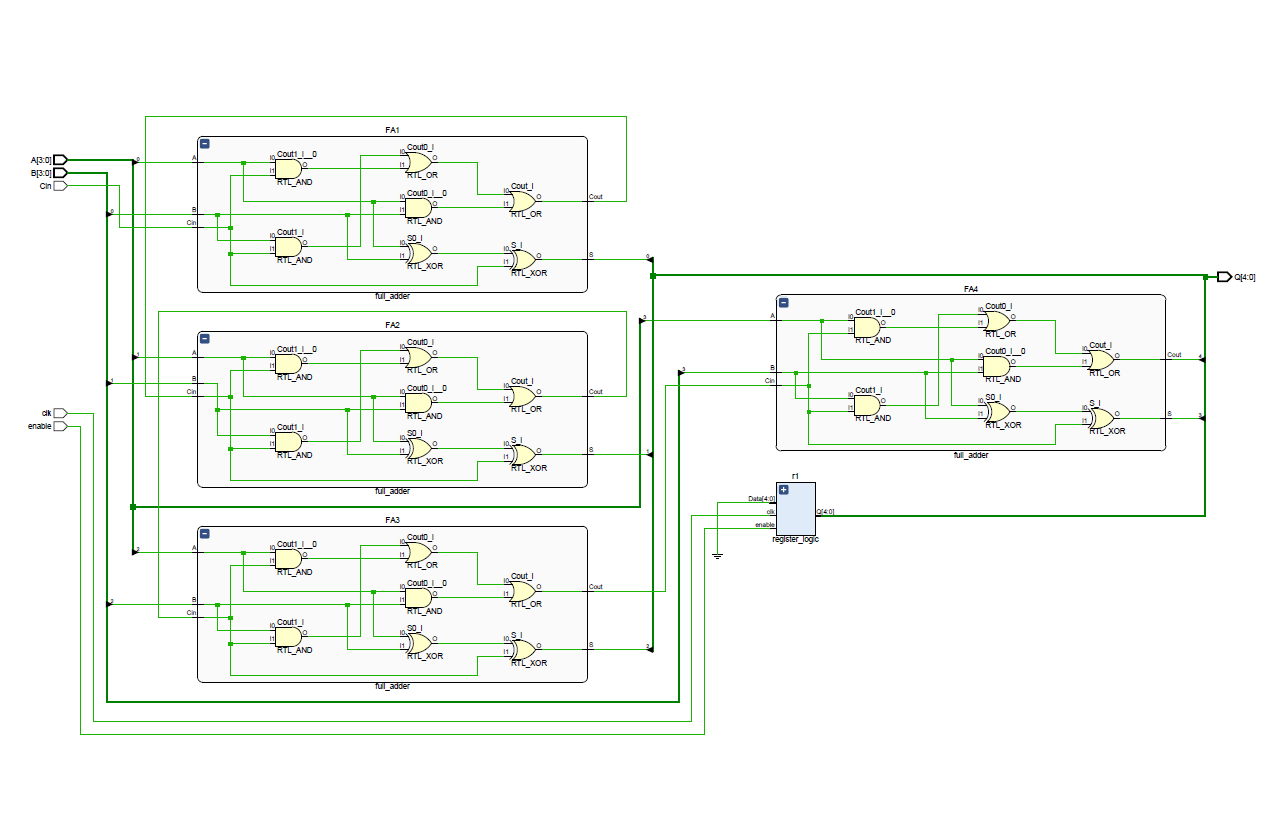
## Simulation Waveform for CLA TB



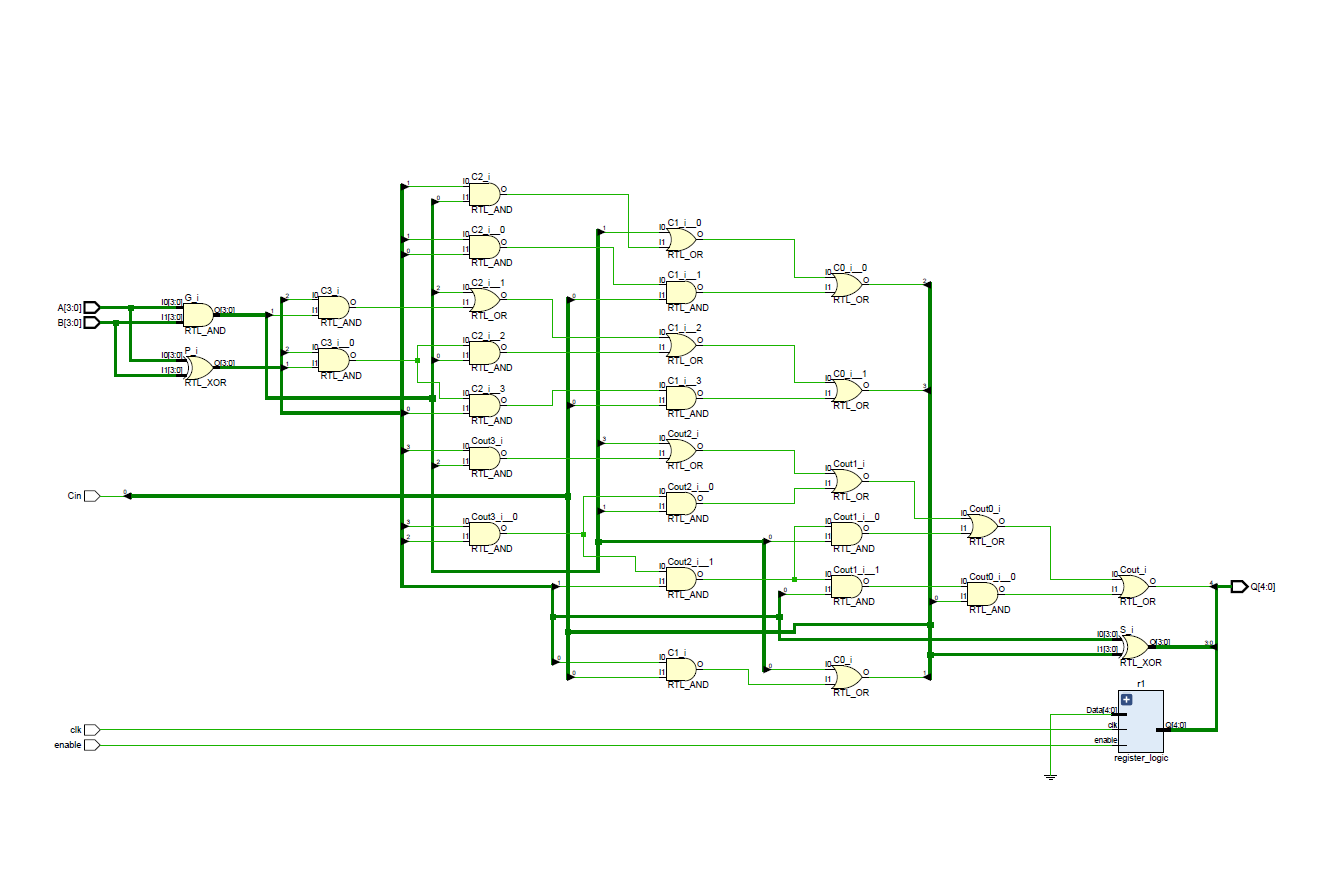
# Part 3 – Speed and Area Comparison of RCA vs. CLA

## Screenshots of Gate-Level Schematics

### RCA



### CLA



## Delay and Area Calculations

### RCA

There are 4 full adders each with 3 AND, 2 OR, and 2 XOR gates. The areas for these gates are 4, 4, and 6 respectively. This means the total area comes for the equation: units of area.

The critical path through our full adder design is the path for each full adder. This means going through an AND gate, then 2 OR gates. The time take for each full adder is , this multiplied by 4 since there are 4 full adders to go through means the critical path would take .

### CLA

My CLA design has 20 AND, 10 OR, and 8 XOR gates. Multiplied by their areas this gives us the following equation: units of area.

The critical path through the carry adder is through 1 XOR, 4 AND, and 2 OR gates. This gives us the following time equation .

## RCA and CLA Delay and Area Analysis

The RCA design has a smaller area footprint but takes a lot longer than the CLA design. The CLA design has the converse, with a larger area but a lesser critical path. This means in space constrained design I would implement the RCA, but in a time constrained design I would implement the CLA.